5. (Amended) The semiconductor device comprising:

a semiconductor substrate;

an isolation insulating film selectively located in a surface of said semiconductor substrate; and

first and second transistors located respectively on first and second active regions which are defined by said isolation insulating film,

said first transistor having a first gate insulating film of a first thickness which is selectively located on said first active region,

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said second transistor having a second gate insulating film of a second thickness which is selectively located on said second active region,

said first thickness being greater than said second thickness,

said isolation insulating film having a recessed portion in an edge portion on the side of said first active region,

said recessed portion being located around said first active region,

a depth of said recessed portion is defined as a vertical height between a main surface of said first active region and a deepest part of said recessed portion, and is not less than 10 nm.

REMARKS

Favorable reconsideration of this application as presently amended in light of the following discussion is respectfully requested.

After entry of the foregoing amendment, Claims 5-9 and 11-13 remain pending in the present application. Claims 1-4 and 10 have been canceled. Claim 5 has been amended to

place it in independent form, thus it is respectfully submitted that the scope of this claim has not been narrowed.[1] No new matter has been added.

By way of summary, the Official Action presents the following issues: The title is objected to as not being indicative of the invention to which the claims are directed; Claims 1-3 and 10 stand rejected under 35 U.S.C. § 112, second paragraph; Claims 1-2 and 4 stand rejected under 35 U.S.C. § 102 as being anticipated by Applicants' admitted prior art; Claims 1-5, 7-11 and 13 stand rejected as being obvious over Feng (U.S. Patent No. 6,417,037) in view of Lee et al. (U.S. Patent No. 6,500,726, hereainafter Lee). Claims 6 and 12 have been identified by the Examiner as reciting allowable subject matter.

As Claims 1-4 and 10 have been canceled, Applicants submit that the rejections pertaining to the claims has been rendered moot.

Applicants thank the Examiner for the courtesy of an interview extended to Applicants' representative on April 24, 2003. During the interview, the rejections noted in the outstanding Official Action were discussed. However, no agreement was reached pending the Examiner's further review on a response as filed. Comments presented during the interview are reiterated below.

REJECTION UNDER 35 U.S.C. § 103

The Official Action has rejected Claims 5, 7-9, 11 and 13 as being unpatentable over Feng in view of Lee. The Official Action states that Feng discloses all of the Applicants' claim limitations with the exception of an isolation film having a depth which is defined relative to a characteristic of variation in threshold voltage such that the depth corresponds to a degree wherein the threshold voltage is substantially constant. The Official Action cites

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[1] This comment is made in view of the recent Festo decision which may limit the availability of the Doctrine of Equivalents for narrowing amendments for patentability reasons.

Lee as disclosing this more detailed aspect of the Applicants' invention and states it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the teachings of Feng with Lee to arrive at the Applicants' claims. Applicants respectfully traverse the rejection.

Amended Claim 5 recites, *inter alia*, a semiconductor device including:

> "... said recessed portion being located around said first active region, a depth of said recessed portion is defined as a vertical height between a main surface of said first active region and a deepest part of said recessed portion, and is not less than 10 nm.."

By way of background, semiconductor devices are known to employ MOS transistors with gate insulting films of different thickness such as produced by a dual oxide process. Informing such transistors, insolation insulting films are provided called shallow trench isolation (STI). In employing such a process to form thin film MOS transistors, an excessively removed edge portion, which faces an active region of the transistor, causes a reduction in threshold voltage due to an inverse narrow-channel effect.[2]

In light of the above deficiency in the art, the present invention is presented. With this object in mind, a brief comparison of the claimed invention in view of the cited references is believed to be in order.

Feng discloses a method of forming a semiconductor including a dual gate dielectric similar to the Applicants' admitted prior art shown in in Fig. 35 of the present application.

Lee discloses a method of forming a shallow trench isolation-type semiconductor device. A process is disclosed for forming the semiconductor device in which a "dent" phenomena can be avoided.[3] As shown in Figure 13 of Lee, a pad oxide film (31) is removed

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[2] Application, pages 1-5.

[3] Lee at Column 3, lines 6-13.

in an intermediate step of forming the semiconductor. The top end of the thermo oxide film (37) is removed to a depth within the range of 150 angstroms and preferably 200 angstroms which corresponds to point 5 to two times as much thickness of a silicon oxide film to be formed on the substrate (30) in a subsequent process. The Examiner notes that this range corresponds to 10 nm and has further cited column 4, lines 1-9 detailing this intermediate step in forming the semiconductor process.

Conversely, the Applicants' semiconductor device has a notched region which has a depth is defined as being equal to a depth wherein it is determined that the threshold voltage is substantially constant according to a characteristic of variation in threshold voltage as shown in Figure 13. It is clear from Figure 13 that 5 nm is along the area of the curve in which a great degree of variability, with respect to the threshold voltage is encountered.[4] In the exemplary embodiment of the invention, 10 nm is in the area wherein the threshold voltage remains substantially constant despite slight variations in the depth at 10 nm.

As shown in more detail in Figure 14 of Lee, a buffer insulating film (51) is formed over the entire surface of the substrate (30). Thus, since the edge portion of the upper surface of the substrate in the active region is exposed and the top end of the thermal-oxide film (37) is removed to the above-mentioned depth, oxygen can be sufficiently supplied thereto. In this way, the space which has been formed laterally from the top end of the inner wall of the trench (35) while removing the top end of the thermal-oxide film (37) is filled with a gate insulating film (52).[5]

As can be appreciated, the depth identified by the Examiner as being equivalent to the notch region of Applicants' claims is nothing more than an intermediate step, this region

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[4] Specification at page 21, lines 6-19.

[5] Lee at Column 8, lines 20-32.

being filled with a further material in a subsequent step. Thus, neither Feng nor Lee, alone or in combination, disclose a depth of a recess portion defined as a vertical height between a main surface of a first active region and a deepest part of the recessed portion being less than 10 nm as recited in Applicants' Claim 5 or any claims depending therefrom. Claim 7 recites substantially the same limitations discussed above. Accordingly, Claims 5-9, 11 and 13 are patentably distinguished over the above-identified combination of references.

Accordingly, Applicants' respectfully request that the rejection of Claims 5-9, 11 and 13 under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

Consequently, in view of the foregoing amendment and remarks, it is respectfully submitted that the present application, including Claims 5-9 and 11-13 is definite, patentably distinguished over the prior art, in condition for allowance, and such action is respectfully requested at an early date.

Respectfully submitted,

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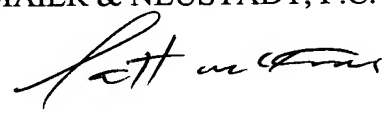

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Amendment Filed on:
6-27-03

IN THE SPECIFICATION

Please amend the specification as follows:

Page 1, line 1, please amend the title to read as follows:

-- SEMICONDUCTOR DEVICE

HAVING A RECESSED ISOLATION INSULTING FILM--

IN THE CLAIMS

Please amend the claims as follows:

1-4. (Canceled)

5. (Amended) [A] The semiconductor device [according to claim 4, wherein] comprising:

a semiconductor substrate;

an isolation insulating film selectively located in a surface of said semiconductor substrate; and

first and second transistors located respectively on first and second active regions which are defined by said isolation insulating film,

said first transistor having a first gate insulating film of a first thickness which is selectively located on said first active region,

said second transistor having a second gate insulating film of a second thickness which is selectively located on said second active region,

said first thickness being greater than said second thickness,

said isolation insulating film having a recessed portion in an edge portion on the side of said first active region,

said recessed portion being located around said first active region,

a depth of said recessed portion is defined as a vertical height between a main surface of said first active region and a deepest part of said recessed portion, and is not less than 10 nm.

10. (Canceled)